JINWEI
JINWEI INTEGRATED CIRCUIT

RIKI Machine Vision Chip

specification

V1. 0–20240401

We are committed to serve every person as a leading global provider of navigation and positioning services based on our homegrown chips

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1. Product Introduction

Figure 1 Product Appearance Diagram

The RIKI machine vision chip is a cost-effective AI terminal product that supports 1T convolutional operations with ultra-low power consumption. It accelerates deep learning inference for edge applications, including machine vision and machine hearing processing, enabling tasks such as detection, recognition, and classification. The chip supports typical network models like face detection, face recognition, human body detection, object detection, and classification.

2. Product Features

1) Supports INT8 quantization and improved computational power

2) Integrated with high-performance ARM cores, supporting secondary development

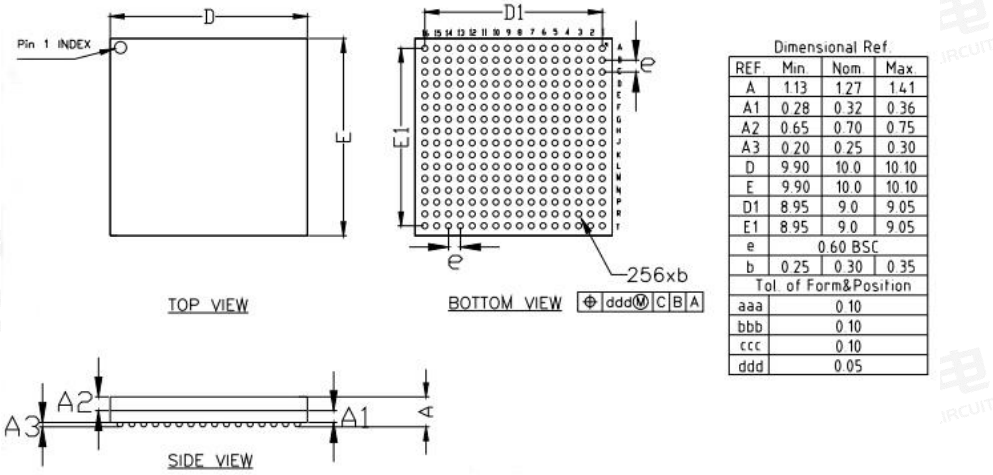
3) Supports mainstream Caffe framewo-rks

4) integrated image preprocessing capabilities

3. Encapsulation Size

The device is packaged in a plastic BGA 256 pin package with a size of 10mm (length) × 10 mm (width) × 1.27mm (height). The external dimensions are shown in the figure below.

Figure 2 Device外形 Dimensions Diagram



Dimensional Ref.

REF.	Min.	Nom.	Max.
A	1.13	1.27	1.41
A1	0.28	0.32	0.36
A2	0.65	0.70	0.75
A3	0.20	0.25	0.30
D	9.90	10.0	10.10
E	9.90	10.0	10.10
D1	8.95	9.0	9.05
E1	8.95	9.0	9.05
e	0.60 BSC		
b	0.25	0.30	0.35
Tol. of Form&Position			
aaa	0.10		
bbb	0.10		
ccc	0.10		
ddd	0.05		

4. Qualification

Table 1 Key Performance Indicators

Characteristic	
Supports INT8 quantization and improved computational power	
Support mainstream neural networks	
High-performance computing power with dual-core 2.0G CPU and up to 1T dedicated neural network processing unit	
Supports integration of 8Gb LPDDR3 memory	
Integrated image preprocessing capabilities	
Superiority	
High performance, low cost, and low power consumption	
High versatility: Supports all mainstream operators, covers common algorithm models, and applies to various scenarios	
Secondary Development: Advanced Software Architecture Facilitates User Secondary Development	
Physical characteristics	
Structure size	10mm×10mm
Encapsulation form	BGA256
Service voltage	Kernel: 0.8V IO: 1.8V or 3.3V
Environment pointer	
Working temperature	-40℃~+85℃
Storage temperature	-40℃~+125℃
Chip interface	
Function Interface (Memory)	2MB Sram
	LPDDR3, up to 2133Mbps
	Supports SD/EMMC

5. Pin Definition

The pin names and descriptions are shown in Figure 2.

Table 2 Device Package Pin Names and Descriptions

Pin number	Pin name	Pin type	Pin function description
A1、T1、C2、D3、P3、E4、G4、J4、N6、P7、N8、P9、N10、P11、N12、P13、M13、L14、N14、T16	VSSH	G	IO power reference ground
C3、D4、F4、K4、P6、N7、P10、N11、K12、M12、K14、P14	VDDH	P	IO high-voltage power input
D5、F5、H5、K5、E6、G6、J6、L6、D7、F7、H7、K7、M7、E8、G8、J8、L8、F9、H9、K9、M9、E10、G10、J10、L10、F11、H11、K11、M11、J12、L12、J13、K13	VSS	G	Core power reference ground
G5、J5、F6、H6、K6、M6、E7、G7、J7、L7、F8、H8、K8、M8、E9、G9、J9、L9、F10、H10、K10、M10、E11、G11、J11、L11	VDD	P	Kernel power supply
R3、H4、E5、D6、P8、N9、P12、L13、N13、M14	VDD18U	P	IO low voltage input
A4、C4、D9、C6、C8、D11、C12、G12、A13、D13、H13、C14、J15、A16	VSSQ	G	DDR reference
B4、C5、C7、D8、D10、D12、H12、C13、G13、B14、D14、J14	VDDQ	P	DDR source
L4、N4、M5、P5	AVSS	G	PLL reference ground
M4、P4、L5、N5	AVDD	P	PLL source
E12、F13	VSSA	G	DDR PLL reference ground
F12、E13	PLLVCCA	P	DDR PLL power supply
C1	STRAPPIN0	I	Configure pin 0
B1	STRAPPIN1	I	Configure pin 1
A2	STRAPPIN2	I	Enable configuration pin 2
R1	SYS_CLK	I	System input clock
R2	SYS_RSTN	I	System reset
M16	PWM	IO	PWM output
T2	CLKOUT_0	O	External clock output
B3	CHIPMODE0	I	Chip operating mode pin 0

Pin number	Pin name	Pin type	Pin function description
B2	CHIPMODE1	I	Chip operating mode pin 1
A3	CHIPMODE2	I	Chip operating mode pin 2
D1	LCDC_PCLK	IO	LCD controller clock
E1	LCDC_VSYNC	IO	LCD controller line synchronization signal
D2	LCDC_HSYNC	IO	LCD controller column synchronization signal
E2	LCDC_DE	IO	Enable LCD controller data
H1	LCDC_R0	IO	LCD controller R0
G3	LCDC_R1	IO	LCD controller R1
G2	LCDC_R2	IO	LCD controller R2
F2	LCDC_R3	IO	LCD controller R3
F3	LCDC_R4	IO	LCD controller R4
G1	LCDC_R5	IO	LCD controller R5
F1	LCDC_R6	IO	LCD controller R6
E3	LCDC_R7	IO	LCD controller R7
K2	LCDC_G0	IO	LCD controller G0
K3	LCDC_G1	IO	LCD controller G1
K1	LCDC_G2	IO	LCD controller G2
J3	LCDC_G3	IO	LCD controller G3
J2	LCDC_G4	IO	LCD controller G4
J1	LCDC_G5	IO	LCD controller G5
H3	LCDC_G6	IO	LCD controller G6
H2	LCDC_G7	IO	LCD controller G7
L1	DVP_CLK	IO	Camera DVP pixel synchronization clock
M1	DVP_VSYNC	IO	Camera DVP frame synchronization signal
L2	DVP_HREF	IO	Camera DVP line sync signal
P2	DVP_DAT0	IO	Camera DVP data 0
P1	DVP_DAT1	IO	Camera DVP Data 1
N3	DVP_DAT2	IO	Camera DVP Data 2
N2	DVP_DAT3	IO	Camera DVP Data 3
N1	DVP_DAT4	IO	Camera DVP Data 4
M3	DVP_DAT5	IO	Camera DVP Data 5
M2	DVP_DAT6	IO	Camera DVP Data 6
L3	DVP_DAT7	IO	Camera DVP Data 7
A11	DDR_DQS[0]	IO	DDR DQS0 differential positive terminal
A12	DDR_DQSN[0]	IO	DDR DQS0 differential negative terminal
A6	DDR_DQS[1]	IO	DDR DQS1 differential positive terminal
A7	DDR_DQSN[1]	IO	DDR DQS1 differential negative terminal
B15	DDR_CSN[0]	O	DDR chip select 0
E16	DDR_CSN[1]	O	DDR Pin 1

Pin number	Pin name	Pin type	Pin function description
C15	DDR_CKE[0]	O	DDR clock enable
B16	DDR_ODT[0]	O	DDR ODT0
D15	DDR_ODT[1]	O	DDR ODT1
A10	DDR_DM_RDQS[0]	O	DDR DM RQDS0
A9	DDR_DM_RDQS[1]	O	DDR DM RQDS1
D16	DDR_CLK	O	DDR positive clock differential
C16	DDR_CLK_N	O	DDR clock differential negative terminal
H16	DDR_ZQ	O	DDR ZQ
E14	DDR_ADDR[0]	O	DDR address 0
E15	DDR_ADDR[1]	O	DDR address 1
F15	DDR_ADDR[2]	O	DDR Address 2
F16	DDR_ADDR[3]	O	DDR address 3
G15	DDR_ADDR[4]	O	DDR address 4
F14	DDR_ADDR[5]	O	DDR address 5
G14	DDR_ADDR[6]	O	DDR address 6
G16	DDR_ADDR[7]	O	DDR address 7
H15	DDR_ADDR[8]	O	DDR address 8
H14	DDR_ADDR[9]	O	DDR address 9
A15	DDR_DQ[0]	IO	DDR data 0
A14	DDR_DQ[1]	IO	DDR Data 1
B13	DDR_DQ[2]	IO	DDR Data 2
B12	DDR_DQ[3]	IO	DDR Data 3
C11	DDR_DQ[4]	IO	DDR Data 4
C10	DDR_DQ[5]	IO	DDR Data 5
B10	DDR_DQ[6]	IO	DDR Data 6
B11	DDR_DQ[7]	IO	DDR Data 7
C9	DDR_DQ[8]	IO	DDR Data 8
B9	DDR_DQ[9]	IO	DDR Data 9
A5	DDR_DQ[10]	IO	DDR Data 10
B8	DDR_DQ[11]	IO	DDR Data 11
A8	DDR_DQ[12]	IO	DDR Data 12
B5	DDR_DQ[13]	IO	DDR Data 13
B6	DDR_DQ[14]	IO	DDR Data 14
B7	DDR_DQ[15]	IO	DDR Data 15
T3	EMMC_CLK	IO	EMMC clock
R4	EMMC_RSTN	O	EMMC reset
T4	EMMC_CMD	IO	EMMC order
T8	EMMC_DAT0	IO	EMMC Data 0
R8	EMMC_DAT1	IO	EMMC Data 1

Pin number	Pin name	Pin type	Pin function description
R7	EMMC_DAT2	IO	EMMC Data 2
T7	EMMC_DAT3	IO	EMMC Data 3
T6	EMMC_DAT4	IO	EMMC Data 4
R6	EMMC_DAT5	IO	EMMC Data 5
R5	EMMC_DAT6	IO	EMMC Data 6
T5	EMMC_DAT7	IO	EMMC Data 7
R9	SD_CD	IO	SD card detection
T9	SD_CLK	IO	SD clock
R10	SD_CMD	IO	SD order
R12	SD_WP	IO	SD write-protect
T10	SD_DAT0	IO	SD Data 0
T11	SD_DAT1	IO	SD Data 1
R11	SD_DAT2	IO	SD Data 2
T12	SD_DAT3	IO	SD Data 3
R14	UART0_TX	IO	UART0 send
T14	UART0_RX	IO	UART0 received
K15	JTAG_TDI	IO	JTAG TDI
L15	JTAG_TDO	IO	JTAG TDO
J16	JTAG_TCK	IO	JTAG TCK
K16	JTAG_TRSTN	IO	JTAG TRSTN
L16	JTAG_TMS	IO	JTAG TMS
P16	GPIOC_0	IO	GPIOC0
N16	GPIOC_1	IO	GPIOC1
N15	GPIOC_2	IO	GPIOC2
M15	GPIOC_3	IO	GPIOC3
R13	I2C0_SCL	IO	I2C clock
T13	I2C0_SDA	IO	I2C data
P15	SPI0_MISO	IO	SPI0 master slave
R15	SPI0_CS0	IO	SPI0 chip select
T15	SPI0_MOSI	IO	SPI0 master slave
R16	SPI0_CLK	IO	SPI0 clock

The mapping diagram of the above pins is shown in Figure 3.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	VSSH	STRAPPIN2	CHIPMODE2	VSSQ	DDR_DQ[10]	DDR_DQS[1]	DDR_DQSN[1]	DDR_DQ[12]	DDR_DM_RDQS[1]	DDR_DM_RDQS[0]	DDR_DQ[0]	DDR_DQSN[0]	VSSQ	DDR_DQ[1]	DDR_DQ[0]	VSSQ
B	STRAPPIN1	CHIPMODE1	CHIPMODE0	VDDQ	DDR_DQ[13]	DDR_DQ[14]	DDR_DQ[15]	DDR_DQ[11]	DDR_DQ[9]	DDR_DQ[6]	DDR_DQ[7]	DDR_DQ[3]	DDR_DQ[2]	VDDQ	DDR_CSN[0]	DDR_ODT[0]
C	STRAPPIN0	VSSH	VDDH	VSSQ	VDDQ	VSSQ	VDDQ	VSSQ	DDR_DQ[8]	DDR_DQ[8]	DDR_DQ[4]	VSSQ	VDDQ	VSSQ	DDR_CKE[0]	DDR_DDR_CLK[1]
D	LCDC_PCLK	LCDC_HSYNC	VSSH	VDDH	VSS	VDD18U	VSS	VDDQ	VSSQ	VDDQ	VSSQ	VDDQ	VSSQ	VDDQ	DDR_ODT[1]	DDR_DDR_CLK
E	LCDC_VSYNC	LCDC_DE	LCDC_R7	VSSH	VDD18U	VSS	VDD	VSS	VDD	VSS	VDD	VSSA	PLLVCCA	DDR_ADDR[0]	DDR_ADDR[1]	DDR_CSN[1]
F	LCDC_R6	LCDC_R3	LCDC_R4	VDDH	VSS	VDD	VSS	VDD	VSS	VDD	VSS	PLLVCCA	VSSA	DDR_ADDR[5]	DDR_ADDR[2]	DDR_ADDR[3]
G	LCDC_R5	LCDC_R2	LCDC_R1	VSSH	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSSQ	VDDQ	DDR_ADDR[6]	DDR_ADDR[4]	DDR_ADDR[7]
H	LCDC_R0	LCDC_G7	LCDC_G6	VDD18U	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDDQ	VSSQ	DDR_ADDR[9]	DDR_ADDR[8]	DDR_ZQ
J	LCDC_G5	LCDC_G4	LCDC_G3	VSSH	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VSS	VDDQ	VSSQ	JTAG_TCK
K	LCDC_G2	LCDC_G0	LCDC_G1	VDDH	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDDH	VSS	VDDH	JTAG_TDI	JTAG_TRSTN
L	DVP_CLK	DVP_HREF	DVP_DAT7	AVSS	AVDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD18U	VSSH	JTAG_TDO	JTAG_TMS
M	DVP_VSYNC	DVP_DAT6	DVP_DAT5	AVDD	AVSS	VDD	VSS	VDD	VSS	VDD	VSS	VDDH	VSSH	VDD18U	GPIOC_3	PWM
N	DVP_DAT4	DVP_DAT3	DVP_DAT2	AVSS	AVDD	VSSH	VDDH	VSSH	VDD18U	VSSH	VDDH	VSSH	VDD18U	VSSH	GPIOC_2	GPIOC_1
P	DVP_DAT1	DVP_DAT0	VSSH	AVDD	AVSS	VDDH	VSSH	VDD18U	VSSH	VDDH	VSSH	VDD18U	VSSH	VDDH	SPI0_MISO	GPIOC_0
R	SYS_CLK	SYS_RSTN	VDD18U	EMMC_RSTN	EMMC_DAT6	EMMC_DAT5	EMMC_DAT2	EMMC_DAT1	SD_CD	SD_CMD	SD_DAT2	SD_WP	I2C0_SCL	UART0_TX	SPI0_CS0	SPI0_CLK
T	VSSH	CLKOUT_0	EMMC_CLK	EMMC_CMD	EMMC_DAT7	EMMC_DAT4	EMMC_DAT3	EMMC_DAT0	SD_CLK	SD_DAT0	SD_DAT1	SD_DAT3	I2C0_SDA	UART0_RX	SPI0_MOSI	VSSH

Figure 3 Block Diagram of the Pin Mapping Function Principle

6. Product Label

The product identification diagram is shown in Figure 4.

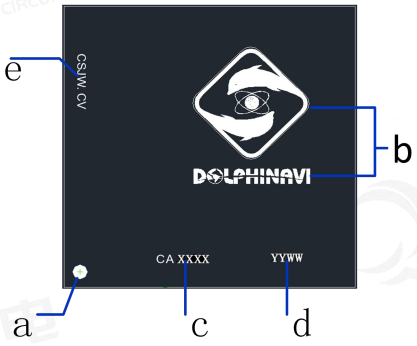


Figure 4 Product Identification

a—— anchor point；

b-The identification mark of the contractor;

c-Batch code;

d-Date code;

e—Device model.

Revision History Record of Revision

Order number	Documentation Edition	Revision	Date of issue
1	V1.0	Found	2024.4

Do It Well.

Changsha Jinwei Integrated Circuit Co., Ltd.
CHANGSHA JINWEI INTEGRATED CIRCUIT CO.,LTD.

corporate headquarters

Address: 5,6,7,11 Floor, Building 14, Phase II, Xincheng Science Park, No.662 Qingshan Road, Changsha High-tech Development Zone

Beijing Branch

Address: Zhongguancun Software Park, Haidian District, Beijing

Guangzhou Branch

Address: Building F, Anju Bao Science and Technology Park, No.8 Qiyun Road, Huangpu District, Guangzhou

contact way

Postal code: 410011

Fax: 0731-82906690

Tel: 0731-82906659

Data acquisition

Website:https://www.cs-jinwei.com